IT IS CLAIMED:

1. A method of storing data, comprising:

utilizing dielectric material positioned within memory cells for non-volatile charge storage that affect an operating parameter of the individual memory cells according to a level of charge stored in at least one common region thereof extending over less than an entire channel of the memory cells,

defining more than two values of said operating parameter that result from more than two levels of charge stored in said at least one common region of the dielectric material in individual cells, thereby to store more than one bit of data in said at least one common region of the dielectric material, and

measuring the level of the memory cells' operating parameter, thereby to read the more than one bit of data stored in individual cells.

2. The method of claim 1, wherein said more than two levels of charge stored in common regions of individual ones of the dielectric material are exactly four levels of charge, thereby to provide exactly four values of said operating parameter to store exactly two bits of data in individual ones of the common regions.

3. The method of claim 1, wherein said more than two levels of charge stored in common regions of individual ones of the dielectric material are more than four levels of charge, thereby to provide more than four values of said operating parameter to store more than two bits of data in individual ones of the common regions.

4. The method of claim 1, wherein measuring the memory cells' operating parameter includes measuring a level of current flowing through the individual memory cells with a fixed voltage on a control gate.

5. The method of claim 1, wherein measuring the memory cells' operating parameter includes measuring a level of voltage on a control gate that causes a

level of current flowing through the individual memory cells to reach a predetermined value.

6. The method of claim 1, wherein utilizing dielectric material includes utilizing a layer of silicon nitride.

7. The method of claim 1, wherein utilizing dielectric material includes utilizing a layer of silicon rich silicon dioxide.

8. The method of claim 1, wherein utilizing dielectric material includes positioning said dielectric material over a portion of a channel of the individual memory cells in series with a select transistor.

9. The method of claim 1, wherein utilizing dielectric material includes positioning said dielectric material over two regions of a channel of the individual memory cells in series with a select transistor in between said two channel regions.

10. A method of operating a non-volatile memory of a type including an array of memory cells that individually has a charge storage dielectric positioned between a conductive gate electrode and a surface of a substrate within a semi-conducting channel that extends across the surface between source and drain regions, comprising:

programming selected ones of the cells by applying voltages to their gates, sources and drains sufficient to transfer electron charge into a common region of their charge storage dielectric to a level that adjusts a threshold of a defined portion of their individual channels to one of more than two threshold levels corresponding to the data being programmed, thereby to store more than one bit of such data in the dielectric common region of individual ones of the cells, and

reading selected ones of the cells by applying voltages to their gates, sources and drains to generate a parameter that is related to the programmed one of more than two threshold levels of the individual cells.

11. The method of claim 10, wherein said more than two threshold levels includes exactly four threshold levels, thereby to store exactly two bits in the common dielectric region of the individual cells.

12. The method of claim 10, wherein said more than two threshold levels includes more than four threshold levels, thereby to store more than two bits in the common dielectric region of the individual cells.

13. A non-volatile memory of a type including an array of memory cells that individually has a charge storing dielectric material positioned between a conductive gate electrode and a surface of a substrate within a semi-conducting channel that extends across the surface between source and drain regions, comprising:

programming means including voltage sources connectable with the gates, sources and drains for transferring charge to at least one defined region of the charge storing dielectric of individual addressed ones of the memory cells to levels that adjust a threshold of at least one defined portion of their individual channels to one of more than two threshold levels corresponding to the data being programmed, thereby to store more than one bit of such data in the dielectric storage material of individual ones of the cells, and

reading means including voltage sources and sense amplifiers connectable with the gates, sources and drains for generating a parameter that is related to the programmed one of more than two threshold levels of the individual cells.

14. A non-volatile memory, comprising:

source and drain diffusions spaced apart across a substrate surface to define lengths of channel regions therebetween,

conductive gates individually positioned over at least a portion of the individual channels,

dielectric charge storage material positioned between the conductive gates and the substrate surface within the channel regions,

a programming circuit including a source of voltages connectable to the diffusions and gates that causes electrons to be transferred from the substrate into regions

of the charge storage dielectric occupying less than the channel length to one of more than two defined ranges according to data being programmed, and

a reading circuit including sense amplifiers connectable to at least the diffusions for identifying one of more than two defined ranges of charge stored in individual charge storage regions.

15. The memory of claim 14, wherein the charge storage dielectric includes silicon nitride.

16. The memory of claim 14, wherein the charge storage dielectric includes silicon rich silicon dioxide.

17. The memory of claim 14, wherein said more than two defined ranges includes exactly four ranges of charge.

18. The memory of claim 14, wherein said more than two defined ranges includes more than four ranges of charge.

19. A non-volatile memory system, comprising:

an array of memory cells, wherein the individual memory cells include:

a channel having a length extending between source and drain regions within a substrate surface,

at least first and second conductive gates positioned over different portions of the channel along its length, and

at least first and second storage elements of dielectric charge trapping material sandwiched between respective ones of said at least first and second control gates,

a programming circuit including a source of voltages connectable to the source and drain regions and to at least first and second gates that causes electrons to be transferred from the substrate into said at least first and second storage elements to a level according to data being programmed, and

a reading circuit including a sense amplifier connectable to at least one of the source and drain regions for determining a single level of charge stored in each of said at least first and second storage elements.

20. The memory system of claim 19, wherein said at least first and second storage elements are formed from the charge trapping material extending continuously between the source and drain regions.

21. The memory system of claim 19, wherein the individual memory cells include a select transistor gate positioned between said at least first and second storage elements and coupled with the channel through a gate dielectric sandwiched therebetween.

22. The memory system of any one of claims 19 - 21, wherein the programming circuit includes a source of voltages that causes electrons to be transferred into said at least first and second storage elements to one of more than two defined ranges according to more than one bit of data being stored, and wherein the reading circuit includes sense amplifiers connectable to at least the source or the drain for identifying levels of charge within one of more than two defined ranges stored in each of said at least first and second charge storage elements.

23. A non-volatile memory, comprising

elongated source and drain diffusions formed in a semiconductor substrate with their lengths extending in a first direction thereacross and being spaced apart in a second direction, the first and second directions being perpendicular to each other, thereby defining memory cell channels in the substrate between adjacent diffusions,

conductive control gates having lengths extending in the first direction, being positioned in the second direction over channel regions immediately adjacent the diffusions and being spaced apart in the second direction over an intermediate region of the cell channels,

dielectric storage material positioned at least between the control gates and a surface of the substrate within the memory cell channels, thereby to form two storage transistors in the cell channels adjacent the diffusions, and

conductive word lines having lengths extending in the second direction and being spaced apart in the first direction, the word lines further being positioned over the control gates and extending therebetween over the intermediate channel regions to provide gates for select transistors in the channels between the two storage transistors.

24. The non-volatile memory of claim 23, which additionally comprises:

a programming circuit including a source of programming voltages connectable to the diffusions, control gates and word lines for adding charge to regions of the dielectric storage material in one of more than two defined charge storage levels according to data being stored, and

a reading circuit including sense amplifiers connectable to at least the diffusions for identifying one of more than two defined ranges of charge stored in individual charge storage regions.

25. The non-volatile memory of claim 24, wherein the programming circuit operates to transfer charge into said more than two defined ranges within a common region the dielectric material.